SPECIFICATION

At page 6, line 1, replace the existing paragraph with the following.

—Figure 10 is a top view of an embodiment of a memory system 1000 according to the present invention. The system 1000 is substantially similar to the system 900 with the addition of a memory module 7[[0]]16. The memory module 716 operates substantially as described earlier with reference to Figure 7. The memory module 716 includes a PLL 720 that is capable of generating a first clock 1stCLK responsive to the system clock CLK and a module board 706. The PLL 720 provides the 1stCLK signal to its corresponding memory devices 708 on the memory module 716. By adding the PLL 720, the system 1000 avoids having to route the system clock separately to each memory device 508, 708 from the memory controller 504. In another embodiment, the PLL 520, 720 might likewise be replaced with a delay locked loop (DLL) that operates similarly to the PLL 520, 720. That is, the DLL is capable of generating the 1stCLK responsive the system clock CLK and to provide the 1stCLK to its corresponding memory devices 508, 708.—